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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,773	08/06/2003	Takeshi Uchitomi	T&A-120	6847

24956 7590 06/14/2006

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EXAMINER	
LE, LANA N	

ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 06/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,773	UCHITOMI ET AL.	
	Examiner	Art Unit	
	Lana N. Le	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 5-9* is/are rejected.

7)☒ Claim(s) *3,4,10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

2. Claims 1-2 and 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin et al (US 6,735,422) in view of Mo et al (US 2004/0,219,884).

Regarding claim 1, Baldwin et al disclose a device (device 201 of fig. 4 which frequency converts via mixer 301 similar to I, Q mixer 273, 275 of fig. 2) a received signal into a baseband to output the signal as an I signal and a Q signal, comprising:

an external input terminal (input terminal at block 297) to which an adjustment signal (calibrating signal from calibration block 401), giving instructions to adjust output-voltage levels of the I signal and the Q signal of a calibrated DC compensating system for the transceiver of figure 2 (col 5, line 65 – col 6, line 18), is inputted (col 18, lines 30-46). Baldwin et al do not disclose a semiconductor integrated circuit device for RF processing in figure 4. Baldwin et al disclose an IC for ZIF transceiver 201 and an IC for baseband processor 203 (fig. 2; col 7, lines 45-62). Mo et al disclose a semiconductor integrated circuit device for RF processing (paragraphs 20-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate

the semiconductor circuit device for RF processing in order to miniaturize the transceiver containing the elements of figure 4 of Baldwin et al and to avoid expensive cost of manufacturing as suggested by Mo et al (para. 20).

Regarding claim 2, Baldwin et al and Mo et al disclose the integrated circuit device according to claim 1, further comprising an output-voltage adjustment unit (307) for adjusting the output-voltage levels of the I signal and the Q signal, based on an adjustment signal inputted via the external input terminal (col 18, lines 37-46).

Regarding claim 4, Baldwin et al and Mo et al disclose the semiconductor integrated circuit device according to claim 3, wherein the voltage outputted from the voltage generator unit (401) is changed in a step of about 0.1 V or less (adjusted values; col 18, lines 38-46).

Regarding claim 5, Baldwin et al disclose a semiconductor integrated circuit device for RF processing, which frequency-converts (via 265, 267) a received signal into a baseband to output the signal as an I signal and a Q signal (fig. 2), comprising:

an external input terminal (input terminal at block 297) to which a reference voltage (predetermined voltage), giving the instruction for adjusting output-voltage levels of the I signal and Q signal (adjusting voltage values of I,Q signal to amplifier 307 representing operation of I, Q amplifiers 273, 275 of figure 2), is inputted (col 5, line 65 – col 6, line 18); and

an amplifier (307 representing operation of I, Q amplifiers 273, 275) for adjusting the output-voltage levels of the signal and Q signal, based on the reference voltage inputted via the external input terminal (col 13, lines 49-51).

Regarding claim 6, Baldwin et al disclose a device for baseband processing (203; fig. 4), which converts, into digital signals (via ADC 313; fig. 4), an I signal and a Q signal (I, Q signal of fig. 2 with calibration compensation system of fig. 4; col 5, line 65 – col 6, line 18) frequency-converted by a semiconductor integrated circuit device for RF processing (201) and measures levels (calibrates voltage levels) of the digital signals (output of ADC 313) to perform level control (col 18, lines 30-46), comprising:

an external output terminal (output terminal from external block 401 to block 297 of RF transceiver 201) for outputting an adjustment signal (voltage or gain adjust signal GAdj) giving instructions to adjust output-voltage levels of the I signal and Q signal (col 13, lines 30-66).

Regarding claim 7, Baldwin et al and Mo et al disclose the semiconductor integrated circuit device according to claim 6, Baldwin et al disclose the device further comprising:

an A/D converter (313) for converting, into digital data, an output-voltage level outputted from the outside (block 203 outside block 201); and a comparison unit (within lookup table 501) for comparing the digital data outputted from the A/D converter (313) and a reference voltage (predetermined voltage), and for outputting the comparison results as an adjustment signal (adjustment signal in memory 405) (col 18, lines 30-46). Baldwin et al do not disclose a semiconductor integrated circuit device for baseband processing and a semiconductor integrated circuit device for RF processing. Mo et al disclose a semiconductor integrated circuit device for baseband processing (para. 22) and a semiconductor integrated circuit device for RF processing (paras. 20-21). It

would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the semiconductor circuit device into chips for RF processing and baseband processing in order to avoid expensive cost of manufacturing as suggested by Mo et al (para. 20).

Regarding claim 8, Baldwin et al disclose a portable terminal system (wireless communication device), comprising:

a first device for RF processing (201), which frequency-converts a received signal into a baseband to output the signal as an I signal and a Q signal; and

a second device for baseband processing (203), which converts, into digital signals (via 313), the I signal and Q signal frequency-converted (via 273, 275; col 13, lines 49-51) by the first device and measures levels (calibrates voltage levels via 401) of the digital signals (output of ADC 313) to perform level control, wherein the first device (201) includes an external input terminal (external input terminal from external block 401) to which an adjustment signal, giving instructions to adjust output-voltage levels of the I signal and Q signal, is inputted (col 18, lines 30-66);

and wherein the second device (203) includes an external output terminal (output terminal to external block 297) for outputting the adjustment signal to the external input terminal of the first semiconductor integrated circuit device (col 18, lines 30-66). Mo et al disclose a first semiconductor integrated circuit device for baseband processing (para. 22) and a second semiconductor integrated circuit device for RF processing (para. 20-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the semiconductor circuit device into chips for RF

processing and baseband processing in order to avoid expensive cost of manufacturing as suggested by Mo et al (para. 20).

Regarding claim 9, Baldwin et al and Mo et al disclose the portable terminal system according to claim 8, wherein Baldwin et al disclose the first semiconductor integrated circuit device includes:

an output voltage adjustment unit (307) for adjusting the output voltage levels of the I signal and the Q signal, based on the adjustment signal inputted via the external input terminal (input terminal at block 297), and the second semiconductor integrated circuit device includes:

an A/D converter (313) for converting, into digital data, an output-voltage level outputted from the outside (from outside block 307, 311 external to 203); and a comparison unit (within LUT 501) for comparing the digital data outputted from the A/D converter (313) and a reference voltage (predetermined voltage) and for outputting the comparison results as an adjustment signal (col 18, lines 30-66).

Allowable Subject Matter

3. Claims 3-4 and 10-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 3, Baldwin et al disclose the semiconductor integrated circuit device according to claim 2, wherein Baldwin et al disclose a control unit (inherent

within 401) for outputting control data (PGM) based on instructions of the adjustment signal; a storage unit (memory 405; fig. 4) for storing the control signal of the control unit (col 18, lines 30-46). Baldwin et al and the cited prior art do not disclose the output-voltage adjustment unit further comprises:

a voltage generator unit for carrying a current with an optional current value among a plurality of different current values and converting the current into an optional voltage, based on the control signal stored in the storage unit; and

an amplifier for outputting a value of the voltage converted by the voltage generator unit, as the output voltage levels of the I signal and Q signal.

Regarding claim 10, Baldwin et al and Mo et al disclose the portable terminal system according to claim 9, wherein Baldwin et al disclose the output-voltage adjustment unit (401) of the first semiconductor integrated circuit device includes:

a control unit (inherent within 401) for outputting control data (PGM) based on instructions of the adjustment signal; a storage unit (memory 405; fig. 4) for storing the control signal of the control unit (col 18, lines 30-46).

However, Baldwin et al, Mo et al, and the cited prior art fail to disclose:

a voltage generator unit for carrying a current with an optional current value among a plurality of different current values and for converting the current into an optional voltage, based on the control signal stored in the storage unit; and

an amplifier for outputting a value of the voltage converted by the voltage generator unit, as output-voltage levels of the I signal and Q signal.

Response to Arguments

4. Applicant's arguments filed 3/16/06 have been fully considered but they are not persuasive. Applicant states there is no external input terminal, however, the device 201 of the main cited reference, Baldwin et al, disclose a ZIF transceiver block 201 receiving an external input signal from exterior blocks 297 and 401 which are outside of ZIF transceiver block 201 (col 5, line 65 - col 6, line 18 where fig. 2 initially shows the transceiver block 201; see also col 7, lines 53-56 where ZIF transceiver block 201 is described in detail). Mo et al (fig. 1; also shown in figure 2 is the receiver 30 and transmitter 32 integrated within a block with input terminal 112, 200, 202 and output terminals 144, 146 and 220; the provisional application 60/445,525 couldn't be ordered was and is not available to the examiner for review only the copending application 10/773,804 with provisional application 60/445,563 is available wherein the IC of figure 1 is not disclosed) was combined for the well known and notoriously old fact that the ZIF transceiver block 201 can be integrated into an IC.

Also, in figure 2 of the Baldwin et al reference, an IC is disclosed for the ZIF transceiver 201 and an IC for the baseband processor 203 (col 7, lines 45-62) which would be obvious to have the ZIF transceiver 201 of figure 4 be implemented into an IC as well. Therefore, the combination of Baldwin et al and Mo et al or Baldwin et al alone for the modified semiconductor IC device for RF processing satisfies the claimed invention and the rejection filed 12/16/05 stands rejected as set forth in the previous office action.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lana N. Le whose telephone number is (571) 272-7891. The examiner can normally be reached on M-F 9:30-18:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F. Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Lana Le

6-05-06

LANA LE
PRIMARY EXAMINER